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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,817	11/02/2001	Hung T. Nguyen	01-629	6850
24319	7590	06/30/2004	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 LEGAL MILPITAS, CA 95035				TSAI, HENRY
ART UNIT		PAPER NUMBER		
		2183		

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,817	NGUYEN, HUNG T.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11/02/01.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-23 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 11/02/01 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description:

"122" (at page 17, line 23);
"235" (at page 20, line 23); and
"302" (at page 28, line 9).

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

at page 19, line 8, "control" should read -decode-;

at page 21, line 20, "control" should read -decode-;

at page 27, lines 13, 15, and 18, "234" should read -233-;

and

at page 28, lines 8 and 19, "234" should read -233-;

Appropriate correction is required.

Claim Objections

3. Claims 4, 12, and 20 are objected to because of the following informalities:

In claim 4, line 3, it is not clear what is meant by "call instruction a fetch/decode". "call instruction a fetch/decode" should read - call instruction, a fetch/decode-. Similar problems exist in claims 12 and 20.

Appropriate correction is required.

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Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. (U.S. Patent No. 5,832,292) (hereafter referred to as Nguyen et al.'292).

Referring to claims 1, 9, and 17, Nguyen et al.'292 discloses, as claimed, for use in a wide-issue pipelined processor (100, see Fig. 1, and see also Col. 2, line 5-7), a mechanism for reducing pipeline stalls between nested calls, comprising: a program counter (PC) generator (366, see Fig. 3, and see also Col. 17, lines 15-17) that generates return PC values for call instructions (see Col. 17, lines 42-44, and return address bus 352 in Fig. 3) in a pipeline of said processor; and return PC Storage (the registers in the prefetch PC control unit 364, see Col. 17, lines 19-21; or special registers 412, see Col. 18, lines 49-53 and Fig. 4), coupled to said PC generator (366, see Fig. 3, and see also Col. 17, lines

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15-17) and located in an execution core said processor (100, see Fig. 1), that stores said return PC values (in the registers in the prefetch PC control unit 364, see Col. 17, lines 19-21; or in special registers 412, see Col. 18, lines 49-53 and Fig. 4) and makes ones of said return PC values available to a PC of said processor execution of corresponding return instructions (see also Col. 16, lines 7-21). Note as set forth in claim 1, Nguyen et al.'292 also discloses the method steps described in claim 9. As to claim 17, in addition to claim 1, Nguyen et al.'292 also discloses a digital signal processor (see Col. 4, lines 23-27), comprising: a pipeline having stages capable of executing call instructions; a wide-issue instruction issue unit (issuer 498, se Fig. 5).

As to claims 2, 10, and 18, Nguyen et al.'292 also discloses: said PC generator (366, see Fig. 3, and see also Col. 17, lines 15-17) is associated with an instruction issue unit (issuer 498, se Fig. 5) of said processor.

As to claims 3, 11, and 19, Nguyen et al.'292 also discloses: said PC generator (366, see Fig. 3, and see also Col. 17, lines 15-17) generates each of said return PC values in a single clock cycle (see Col. 40, lines 19).

As to claims 4, 12, and 20, Nguyen et al.'292 also discloses: a return PC queue or said return PC storage has (in

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the registers of the prefetch PC control unit 364, see Col. 17,
lines 19-21; or in special registers 412, see Col. 18, lines 49-
53 and Fig. 4) at least as many slots as a number of call
instructions a fetch/decode stage of said pipeline can decode
prior to grouping. Note the prefetch PC control unit 364
comprises many registers, see Col. 17, lines 19-21; and also the
special registers 412, see Col. 18, lines 49-53 and Fig. 4.

As to claims 5, 13, and 21, Nguyen et al.'292 also discloses: said return PC values move through registers of said return PC storage (the registers in the prefetch PC control unit 364, see Col. 17, lines 19-21; or special registers 412, see Col. 18, lines 49-53 and Fig. 4) as corresponding ones of said return instructions move through stages in said pipeline (since the prefetch PC control unit 364 comprises registers storing the return addresses, see Col. 17, lines 19-21; and also the special registers 412, see Col. 18, lines 49-53 and Fig. 4).

As to claims 6, 14, and 22, Nguyen et al.'292 also discloses: said return PC storage (the registers in the prefetch PC control unit 364, see Col. 17, lines 19-21; or special registers 412, see Col. 18, lines 49-53 and Fig. 4) makes said ones of said return PC values available to a PC of said processor (100, see Fig. 1) as said corresponding return

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instructions are in an execution stage of said pipeline (note IFU 102 connected with IEU 104 through 124 and 126 see Fig. 1).

As to claims 7, 15, and 23 Roth et al.'326 also discloses: said call instruction is executed in a fetch/decode stage of said pipeline (since prefetch PC control unit 364 is inside instruction fetch unit 102, see Figs. 1-3).

As to claims 8, and 16, Nguyen et al.'292 also discloses: said processor (100, see Fig. 1) is a digital signal processor (see Col. 4, lines 23-27).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sites et al. discloses high-performance CPU of the RISC (reduced instruction set) type employs a standardized, fixed instruction size, and permits only simplified memory access data width and addressing modes. Truben discloses Method and apparatus for unobtrusively monitoring processor states and characterizing bottlenecks in a pipelined processor executing grouped instructions. Beckwith et al. discloses a high-performance pipelined central processor for predicting the occurrence of executing single-cycle instructions and multicycle instructions. The return address is transferred

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from the stack to the program counter register on the processing cycle immediately following the return prediction, and normal program flow is resumed. Roth et al. teaches a system as shown in Fig. 6 comprising many PC counters 110, 111, 112, and 113 through the pipelined stages.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

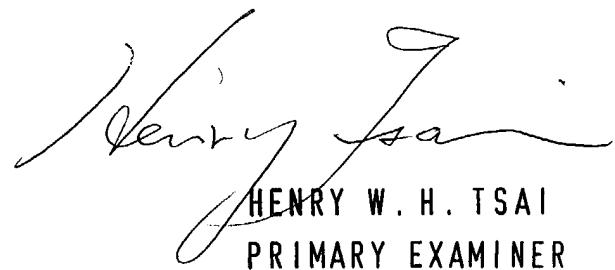
8. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the **Group at fax number: 703-872-9306.**

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This practice may be used for filing papers not requiring a fee.

It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER

June 28, 2004